8 Implementation of Gates

- **I** - Current in cycle
- **R** - Resistance
- **V** - Potential electricity

**Ohm’s Law:** \( I = \frac{V}{R} \)

For example, if Potential is 10V and Resistance is 2\( \Omega \), the current will be 5A.
Voltage division

- If there are two (or more) resistors connected in a line, the total resistance is the sum of the resistances. (In this example the total resistance is 5 Ω).
- In this example the current is 2A. Resistor R feels that it connected to a potential of 6V (I·R). Resistor R1 feels that it connected to a potential of 4V (I·R1).
The cycle from the previous slide can be written as:

\[ 0V \rightarrow R = 3 \, \Omega \rightarrow R_1 = 2 \, \Omega \rightarrow +10V \]

The potential here is 6V.

The real current is of electrons from “-” to “+”, but it is common to write the current from “+” to “-”. No reasonable explanation why Electrical Engineers do this.
Semiconductors

A Silicon infected by Arsenic

A Silicon infected by Aluminum
PN Junction - A diode
Forward biased diode
Reverse biased diode
Most of the voltage drop is on the resistor

Most of the voltage drop is on the diode
**AND gate**

**Diagram:**

- Inputs: A, B
- Output

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>0V</td>
<td>~0V</td>
</tr>
<tr>
<td>0V</td>
<td>5V</td>
<td>~0V</td>
</tr>
<tr>
<td>5V</td>
<td>0V</td>
<td>~0V</td>
</tr>
<tr>
<td>5V</td>
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<td>~5V</td>
</tr>
</tbody>
</table>

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**OR gate**

- **Input:** A, B
- **Output:**
  - $0V$
  - $5V$

**Truth Table:**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0V$</td>
<td>$0V$</td>
<td>$\sim0V$</td>
</tr>
<tr>
<td>$0V$</td>
<td>$5V$</td>
<td>$\sim5V$</td>
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</table>
**NPN Transistor**

![Diagram of an NPN Transistor]
Cutoff

- No current from collector to emitter, since current cannot pass from the collector to the base.
Active

- There is a current from collector to emitter, since the barrier (or part of it) between the collector and the base evaporated.
- If more current flows from B to E, the transistor will let more current flow from C to E.
- If the barrier between the collector and the base totally evaporated, the transistor is in saturation.
**NOT gate**

Input: B, C

Output: E

<table>
<thead>
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<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>~5V</td>
</tr>
<tr>
<td>5V</td>
<td>~0V</td>
</tr>
</tbody>
</table>
An implementation of the formula:

\[ A \cdot B + C \]
Clock

+5V

Capacitor

Capacitor

Output

0V

Output

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